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UNITED STATES PATENT APPLICATION

FOR

FIELD EMISSION DEVICE

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FIELD EMISSION DEVICE

[0001] The present application is a Divisional of Application No. 10/160,413, filed May 30, 2002.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] The present invention relates generally to a field emission device having an emitter formed in a nano hole, and more particularly to a field emission device which can lower the operating voltage to reduce the power consumption.

DESCRIPTION OF THE PRIOR ART

[0003] Field emission devices employ a phenomenon that electrons are emitted from a part of the emitter when a voltage is applied between the emitter and a gate electrode. The field emission devices are applied to microwave devices or field emission displays (FED).

[0004] Generally, the field emission device is divided into a diode-type having an upper plate and a lower plate used as an emitter and a cathode, and a triode-type having a gate formed around an emitter for supplying a voltage.

[0005] As the diode-type has a high operating voltage and is difficult to control the amount of electron emission, the triode-type is usually employed. In particular, a spindle type emitter is widely used.

[0006] The spindle type emitter has a fine tip of a cylindrical shape and emits electrons when a high electric field is applied to an end of the fine tip. Thus, as the operating characteristic of the spindle type emitter is stable, it has been most widely used as an emitter of the triode-type field emission device. Further, a lot of researches on the shape and material of the tip have been actively made.

[0007] As the field emission device having this spindle type emitter, however, is driven with a high voltage of about 50V~1OOV, it has a high

consumption voltage. Thus, it is required that the voltage be further lowered in order to commercialize the field emission device using the spindle type emitter.

[0008] In order to fabricate a field emission device driven with a low voltage, an aspect ratio of the emitter must be increased. Therefore, a research on manufacturing the emitter using carbon nanotube has recently been made.

[0009] **Fig. 1** is a cross-sectional view of a conventional field emission device.

[0010] Referring now to **Fig. 1**, an emitter electrode 12 made of metal is formed on a silicon substrate 11. An insulating layer 15 having an aperture 15a is formed on the emitter electrode 12. A catalyst layer 13 made of a transition metal is formed on the emitter electrode 12 exposed through the aperture 15a. An emitter 14 is formed on the catalyst layer 13. A gate electrode 16 having a given pattern is formed on the insulating layer 15. The transition metal includes carbon nanotube, a nano grain film and a metal tip.

[0011] At this time, the emitter 14 composed of a metal tip may be formed right on the emitter electrode 12 exposed through the aperture 15a without the catalyst layer 13.

[0012] If an operating voltage is applied to the emitter electrode 12 and the gate electrode 16, respectively, a high electric field is formed around theemitter 14. Due to this, electrons are emitted from the emitter 14.

[0013] Meanwhile, in order to fabricate the field emission device driven with a low voltage, it is required that the aspect ratio of the emitter be increased. The aspect ratio of the emitter can be increased by a formation of a hole having a nanometer size. The hole having a nanometer size should be formed in anodized aluminum oxide layer since the hole can not be formed in conventional oxide layer. However, anodized aluminum oxide is not suitable for the semiconductor manufacturing process. Therefore, it is difficult to manufacture the emitter having a large aspect ratio by using the conventional method.

SUMMARY OF THE INVENTION

[0014] The present invention is contrived to solve the above problems and an object of the present invention is to provide a field emission device, capable of reducing the driving voltage and thus lower the power consumption, in such as way that a hole having a nanometer size is formed by processes of manufacturing the semiconductor devices and an emitter is then formed in the hole to increase the aspect ratio of the emitter.

[0015] In order to accomplish the above object, a field emission device according to the present invention, is characterized in that it comprises a silicon substrate having an emitter electrode formed in a surface portion thereof, an insulating layer formed on the emitter electrode and having a nano hole to expose the emitter electrode; an emitter formed on the emitter electrode exposed through the nano hole; and a gate electrode formed on the insulating layer.

[0016] A method of fabricating a field emission device according to the present invention is characterized in that it comprises the steps of forming silicon rods on a silicon substrate; forming an emitter electrode within the silicon substrate; forming insulating layer between the silicon rods; forming a gate electrode on the insulating layer; forming a nano hole in the insulating layer by removing the silicon rods; and forming an emitter on the emitter electrode exposed through the nano hole.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

[0018] **Fig. 1** is a cross-sectional view of a conventional field emission device;

[0019] **Fig. 2** is a cross-sectional view of a field emission device according to the present invention;

[0020] **Fig. 3a - Fig. 3g** are cross-sectional views of field emission devices for describing a method of fabricating the field emission devices according to a preferred embodiment of the present invention; and

[0021] **Fig. 4a** and **Fig. 4b** are cross-sectional views of field emission devices for describing a method of fabricating the field emission devices according to another embodiment of the present invention.

DETAILED DESCRIPTION

[0022] The present invention will be described in detail by way of a preferred embodiment with reference to accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

[0023] **Fig. 2** is a cross-sectional view of a field emission device according to the present invention.

[0024] Referring now to **Fig. 2**, an emitter electrode 24 is formed on a silicon substrate 21. An insulating layer 25 is formed on the emitter electrode 24. A nano hole 27 having a nanometer size is formed in the insulating layer 25. A catalyst layer 28 is formed on the emitter electrode 24 exposed through the nano hole 27. An emitter 29 is formed within the nano hole 27. A gate electrode 26 is formed on the insulating layer 25 around the emitter 29.

[0025] The emitter electrode 24 is composed of an impurity region in which an impurity is implanted into the silicon substrate 21. The insulating layer 25 is formed of a low-temperature silicon oxide film or a silicon nitride film. Further, the catalyst layer 28 is made of a transition metal and is formed by means of an Electrochemical Deposition Method.

[0026] The emitter 29 is selectively formed on the catalyst layer 28 by a Chemical Vapor Deposition Method if the emitter 29 is made of either carbon nanotube or a nano grain film. On the contrary, in ease of the emitter 24 is made of a metal tip, the emitter 24 is formed by an Electro-Beam Evaporation Method The gate electrode 26 is made of a common metal or polysilicon.

[0027] A method of fabricating the field emission device formed thus will be below described. **Fig. 3a - Fig. 3g** are cross-sectional views of field emission devices for describing a method of fabricating the field emission devices according to a preferred embodiment of the present invention.

[0028] Referring now to **Fig. 3a**, a given region of a silicon substrate 21 is etched by a given thickness to form a protruded portion 21a.

[0029] By reference to **Fig. 3b**, an oxide film 22 is grown on a surface of the silicon substrate 21 and the protruded portion 21a by an oxidization process. The surface of the silicon substrate 21 is changed to the oxide film 22 as the reaction of silicon with oxygen. At this time, the thickness of the protruded portion 21a remained can be thin to be a nanometer size by controlling the oxidation condition.

[0030] Referring now to **Fig. 3c**, the oxide film 22 is removed to form silicon rods 23 made of the protruded portion 21 a that remains without being oxidized.

[0031] Next, an n-type impurity is implanted into the silicon substrate 21, and then annealing process is performed to diffuse the impurity. Thereby, the emitter electrode 24 is formed in a surface portion of the silicon substrate 21.

[0032] By reference to **Fig. 3d**, an insulating layer 25 is formed between the silicon rods 23. A gate electrode 26 is then formed on a given region of the insulating layer 25. The insulating layer 25 is formed to have the same height to the silicon rod 23, so that an upper surface of the silicon rod 23 is exposed. The gate electrode 26 is formed to have a given pattern so that it does not overlap with the silicon rod 23.

[0033] At this time, a self align etching method can be used to form the gate electrode 26.

[0034] The higher of the insulating layer 25 formed on the silicon rod 23 is higher than that of the insulating layer 25 formed between the silicon rod 23 by the aspect of the silicon rod 23. In this status, a conductive layer and a

photoresist film (not shown) are formed on the insulating layer 25, sequentially. The photoresist film is removed by an etch hack process until the conductive layer formed on the silicon rod 23 is exposed. And then the photoresist film and the conductive layer exposed are removed until the conductive layer formed between the silicon rod 23 is exposed. The gate electrode 26 composed of the conductive layer remained is formed by the above self-aligned patterning method.

[0035] The insulating layer 25 is formed of a low-temperature silicon oxide film or a silicon nitride film. The gate electrode 26 is formed of metal or polysilicon.

[0036] Referring now to **Fig. 3e**, the silicon rod 23 is removed by etching process. A nano hole 27 having a nanometer size is formed at a region from which the silicon rod 23 is removed. The emitter electrode 24 is exposed at the bottom of the nano hole 27.

[0037] A dry etch process or a wet etch process is performed to remove the silicon rod 23. The etching selective ratio of the insulating layer 25 and the silicon rod 23 is controlled to remove only the silicon rod 23.

[0038] Thereafter, an emitter 29 is formed within the nano hole 27. At this time, a method of forming the emitter 29 may differ depending on what material is the emitter is formed. A method of forming the emitter 29 using carbon nanotube or a nano grain film will be first described below. Referring now to **Fig. 3f**, if the carbon nanotube or the nano grain film is used to form the emitter 29, a catalyst layer is required to grow the carbon nanotube or the nano grain film. A catalyst layer 28 is formed on the emitter electrode 24 exposed through the nano hole 27. The catalyst layer 28 is formed by means of an Electrochemical Deposition Method, so that the catalyst layer 28 is selectively formed only on the emitter electrode 24.

[0039] Referring now to **Fig. 3g**, the carbon nanotube or the nano grain film is formed on the catalyst layer 28 to form the emitter 29. The carbon nanotube or nano grain film is grown by means of a Chemical Vapor

Deposition Method. Thereby, the triode-type field emission device can be fabricated.

[0040] As shown in **Fig. 3g**, the aspect ratio of the emitter 29 is increased since the emitter 29 is formed within the nano hole 27. Therefore, electrons can be efficiently emitted even at a low voltage level.

[0041] Meanwhile, a method of forming the emitter 29 using a metal tip will be below described by reference to **Fig. 4a** and **Fig 4b**.

[0042] Referring now to **Fig. 4a**, though not shown in the drawings, processes before **Fig. 4a** are same to those from **Fig. 3a - Fig. 3e**. The process before **Fig. 4a** will not be described. An emitter electrode 24 is grown to form an emitter growth layer 24a at the bottom of a nano hole 27. A sacrifice metal layer 30 is then formed on an insulating layer 25 and a gate electrode 26. The sacrifice metal layer 30 is made of a material that is usually made of aluminum or materials that can be lift off but do not affect other thin films. The sacrifice metal layer 30 is formed by means of an Electro-Beam Evaporation Method.

[0043] Referring now to **Fig. 4b**, metal is deposited within the nano hole 27 using a deposition apparatus having a good linearity to thus form an emitter 31. The sacrifice metal layer 30 is then removed. Thus the triode-type field emission device which can smoothly emit electrons even at a low voltage level is fabricated.

[0044] As mentioned above, the present invention includes forming a hole having a nanometer size by using common semiconductor manufacturing processes and forming an emitter within the nano hole to increase the aspect ratio of the emitter. Therefore, the present invention has outstanding advantages that it can lower the driving voltage and reduce the power consumption

[0045] The present invention has been described with reference to a particular embodiment in connection with a particular application. Those having ordinary skill in the art and access to the teachings of the present invention will recognize additional modifications and applications within the scope thereof.

[0046] It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the present invention.